**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1.–2. (Cancelled).

3. (Previously presented) A distributed multiprocessing computer system, comprising:

a plurality of processors each coupled to an I/O bridge;

a plurality of memory modules coupled one each to the plurality of processors, each memory module able to store data blocks that are shared between said processors, wherein coherence of the shared data blocks is maintained using a directory based coherence protocol;

at least one I/O device coupled to the I/O bridge, the I/O device and I/O bridge performs direct memory access (DMA) to transfer data blocks to the memory modules; and

wherein the I/O bridge obtains exclusive ownership of shared memory module data blocks during I/O device access, and wherein said I/O bridge includes a DMA device that supports both in-order and out-of-order DMA read and write streams of data blocks.

4. (Original) The distributed multiprocessing computer system of claim 3 wherein the DMA device that performs an in-order stream of reads of data blocks always receives coherent data blocks that do not have to be written back to the memory module.

5.-16. (Cancelled).